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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/015,076	10/26/2001	Kalvin E. Williams	01-669 1496.00169	9488

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EXAMINER

LEE, CHRISTOPHER E

ART UNIT	PAPER NUMBER
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2112

DATE MAILED: 05/05/2004

2

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/015,076

Applicant(s)

WILLIAMS ET AL.

Examiner

Christopher E. Lee

Art Unit

2112

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-17 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-4,9-12 and 17 is/are rejected.
- 7) ☒ Claim(s) 5-8 and 13-16 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 26 October 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-4, 9-12 and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Miller [US 4,780,822].

*Referring to claim 1*, Miller discloses a circuit (i.e., integrated circuit having semaphore circuits in the Figure) comprising: a memory element (i.e., storage elements 20, 22, 24 and 26 within the semaphore circuit 10 of the Figure) defining a semaphore allocatable to a resource (See col. 1, lines 7-10; in fact, said storage elements defining semaphore allocated to a shared memory cell); and a controller (i.e., arbiter 28 within the semaphore circuit 10 of the Figure) configured to (i) present a granted status (i.e., the signal developed on the pad 142 in the Figure) in response to a processor reading a first address (i.e., processor reading an appropriate storage element, e.g., storage element 26 within the semaphore circuit 10 of the Figure) while said semaphore has a free status (See col. 5, lines 22-58), (ii) set said semaphore to a busy status in response to presenting said granted status (i.e., the appropriate storage element is written in a low-logic-level, which indicates that the shared memory cell is in use; See the semaphore circuit logic within the semaphore circuit 10 of the Figure), and (iii) present said busy status in response to said processor reading said first address while said semaphore has said busy status (i.e., at once, the appropriate storage element has set to a low-logic-level, the arbiter in the semaphore circuit logic maintains the indication, such that the shared memory cell is in use; See the semaphore circuit logic within the semaphore circuit 10 of the Figure).

*Referring to claim 2*, Miller teaches said controller (i.e., arbiter 28 within the semaphore circuit 10 of the Figure) is further configured to set said semaphore to said free status in response to said processor writing to said first address (See col. 5, lines 59-68; i.e., “write” (a one) into the appropriate storage element indicating that the shared memory cell is no longer in use).

*Referring to claim 3*, Miller teaches said controller (i.e., arbiter 28 within the semaphore circuit 10 of the Figure) is further configured to present said status of said semaphore (i.e., indicating the status of semaphore on the pad 142 in the Figure; busy: low-logic-level signal, free: high-logic-level signal) in response to said processor reading a second address (i.e., processor reading an appropriate storage element, e.g., storage element 22 in the Figure; See col. 5, lines 20-68).

*Referring to claim 4*, Miller teaches said controller (i.e., arbiter 28 within the semaphore circuit 10 of the Figure) is further configured to maintain said status of said semaphore (See the logic of arbiter using two NOR gates in the Figure; i.e., the logic and storage element maintains the status of semaphore) in response to said processor writing to said second address (i.e., processor sets line 114 to “write enable” and send data to the storage element 22 via line 142, and thereafter the semaphore status is maintained by said logic of arbiter according to the semaphore circuit logic in the Figure).

*Referring to claim 9*, Miller discloses a method of allocating a resource to a processor (See Description of the Prior Art in col. 1, lines 10+) comprising the steps of: defining a semaphore allocatable to said resource (See col. 1, lines 7-10; in fact, storage elements defining semaphore allocated to a shared memory cell); presenting a granted status (i.e., the signal developed on the pad 142 in the Figure) in response to said processor reading a first address (i.e., processor reading an appropriate storage element, e.g., storage element 26 within the semaphore circuit 10 of the Figure) while said semaphore has a free status (See col. 5, lines 22-58); setting said semaphore to a busy status in response to presenting said granted status (i.e., the appropriate storage element is written in a low-logic-level, which indicates that the shared memory cell is in use; See the semaphore circuit logic within the semaphore circuit 10 of the

Figure); and presenting said busy status in response to said processor reading said first address while said semaphore has said busy status (i.e., at once, the appropriate storage element has set to a low-logic-level, the arbiter in the semaphore circuit logic maintains the indication, such that the shared memory cell is in use; See the semaphore circuit logic within the semaphore circuit 10 of the Figure).

*Referring to claim 10*, Miller teaches the step of setting said semaphore to said free status in response to said processor writing to said first address (See col. 5, lines 59-68; i.e., “write” (a one) into the appropriate storage element indicating that the shared memory cell is no longer in use).

*Referring to claim 11*, Miller teaches the step of presenting said status of said semaphore (i.e., indicating the status of semaphore on the pad 142 in the Figure; busy: low-logic-level signal, free: high-logic-level signal) in response to said processor reading a second address (i.e., processor reading an appropriate storage element, e.g., storage element 22 within the semaphore circuit 10 of the Figure; See col. 5, lines 20-68).

*Referring to claim 12*, Miller teaches the step of maintaining said status of said semaphore (See the logic of arbiter using two NOR gates in the Figure; i.e., the logic and storage element maintains the status of semaphore) in response to said processor writing to said second address (i.e., processor sets line 114 to “write enable” and send data to the storage element 22 via line 142, and thereafter the semaphore status is maintained by said logic of arbiter according to the semaphore circuit logic within the semaphore circuit 10 of the Figure).

*Referring to claim 17*, Miller discloses a circuit (i.e., semaphore circuit 10 in the Figure) comprising: means for defining a semaphore (i.e., storage elements 20, 22, 24 and 26 in the Figure) allocatable to a resource (See col. 1, lines 7-10; in fact, said storage elements defining semaphore allocated to a shared memory cell); means for presenting a granted status (i.e., means for developing the signal on the pad 142 in the Figure) in response to a processor reading a first address (i.e., processor reading an appropriate storage element, e.g., storage element 26 in the Figure) while said semaphore has a

free status (See col. 5, lines 22-58); means for setting said semaphore (i.e., semaphore circuit) to a busy status in response to presenting said granted status (i.e., the appropriate storage element is written in a low-logic-level, which indicates that the shared memory cell is in use; See the semaphore circuit logic in the Figure); and means for presenting said busy status in response to said processor reading said first address while said semaphore has said busy status (i.e., at once, the appropriate storage element has set to a low-logic-level, the arbiter in the semaphore circuit logic maintains the indication, such that the shared memory cell is in use; See the semaphore circuit logic in the Figure).

#### ***Allowable Subject Matter***

3. Claims 5-8 and 13-16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

4. The following is a statement of reasons for the indication of allowable subject matter:

The limitations of claim 5 and 13 are respectively deemed allowable over the prior art of record as the prior art fails to teach or suggest that a second memory element defining a second semaphore allocatable to said semaphore, i.e., cascaded semaphoring. The claims 6-8 are the dependent claims of the said claim 5, and the claims 14-16 are the dependent claims of the said claim 13.

#### ***Conclusion***

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

##### ***With regard to Hardware Semaphore,***

Dror [US 5,276,886 A] discloses hardware semaphores in a multi-processor environment.

Wenniger [US 6,018,785 A] discloses interrupt-generating hardware semaphore.

Shannon et al. [US 4,380,798] disclose semaphore register including ownership bits.

Takahashi et al. [JP 401321525 A] disclose hardware semaphore.

##### ***With regard to Semaphoring in Multiprocessor system,***

Parks [US 6,594,736 B1] discloses system and method for semaphore and atomic operation management in a multiprocessor.

Tissot [US 5,951,662 A] discloses single latch semaphore register device for multi-processor systems.

Earnshaw et al. [US 5,050,072] disclose semaphore memory to reduce common bus contention to global memory with localized semaphores in a multiprocessor system.

Iacobovici et al. [US 5,696,939 A] disclose apparatus and method using a semaphore buffer for semaphore instructions.

Buch [US 5,669,002 A] discloses multi-processor resource locking mechanism with a lock register corresponding to each resource stored in a common memory.

Falik [US 6,263,425 B1] discloses circuit that implements semaphores in a multiprocessor environment without reliance on atomic test and operations of the processor cores.

Kim [US 2002/0165896 A1] discloses multiprocessor communication system and method.

Kloth [US 6,549,961 B1] discloses semaphore access in a multiprocessor system.

*With regard to Systems using Semaphoring method,*

McDonald et al. [US 6,560,627 B1] discloses mutual exclusion at the record level with priority inheritance for embedded systems using one semaphore.

Saitoh [US 5,634,038 A] discloses common memory protection system in a multiprocessor configuration using semaphore-flags stored at complementary addresses for enabling access to the memory.

Nieuwland et al. [US 6,493,805 B2] disclose method and system for synchronizing block-organized data transfer amongst a plurality of producer and consumer stations.

Schibinger et al. [US 6,389,515 B1] disclose system and method for avoiding deadlocks utilizing split lock operations to provide exclusive access to memory during non-atomic operations.


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 703-305-5950. The examiner can normally be reached on 9:00am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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